

The listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Canceled)

2. (Original) A method for manufacturing a thin film integrated circuit, comprising the steps of:

forming a separation layer over an insulating substrate;

forming at least two thin film integrated circuits over the separation layer;

selectively forming a groove between the two thin film integrated circuits to expose a part of the separation layer and form a connection region which is a part of the two thin film integrated circuits; and

separating the insulating substrate by introducing an etchant into the opening and removing the separation layer,

wherein the two thin film integrated circuits are integrated by the connection region.

3. (Original) A method for manufacturing a thin film integrated circuit, comprising the steps of:

forming a separation layer over an insulating substrate;

forming at least two thin film integrated circuits over the separation layer;

selectively forming a groove between the two thin film integrated circuits to expose a part of the separation layer and form a connection region which is a part of the two thin film integrated circuits;

attaching an antenna substrate provided with an opening and an antenna over the two thin film integrated circuits; and

separating the insulating substrate by introducing an etchant into the groove and the opening and removing the separation layer,

wherein the two thin film integrated circuits are integrated by the antenna substrate.

4. (Canceled)

5. (Previously Presented) The method for manufacturing a thin film integrated circuit according to claim 2, further comprising the step of:

attaching an antenna to the two thin film integrated circuits.

6. (Original) The method for manufacturing a thin film integrated circuit according to claim 2, further comprising the steps of:

attaching an antenna to the two thin film integrated circuits; and

attaching the two thin film integrated circuits to a flexible substrate.

7. (Previously Presented) The method for manufacturing a thin film integrated circuit according to claim 3, further comprising the step of:

attaching the two thin film integrated circuits to a flexible substrate.

8. (Canceled)

9. (Original) The method for manufacturing a thin film integrated circuit according to claim 2,

wherein each of the thin film integrated circuits comprises a thin film transistor and an insulating film containing nitrogen provided over and under the thin film transistor.

10. (Original) The method for manufacturing a thin film integrated circuit according to claim 3,

wherein each of the thin film integrated circuits comprises a thin film transistor and an insulating film containing nitrogen provided over and under the thin film transistor.

11. (Canceled)

12. (Original) The method for manufacturing a thin film integrated circuit according to claim 2,

wherein the etchant is a gas or a liquid including halide typified by  $\text{ClF}_3$ .

13. (Original) The method for manufacturing a thin film integrated circuit according to claim 3,

wherein the etchant is a gas or a liquid including halide typified by  $\text{ClF}_3$ .

14. (Canceled)

15. (Original) The method for manufacturing a thin film integrated circuit according to claim 2,

wherein the insulating substrate is a glass substrate, a quartz substrate, or a substrate made of a synthetic resin such as plastic or acrylic.

16. (Original) The method for manufacturing a thin film integrated circuit according to claim 3,

wherein the insulating substrate is a glass substrate, a quartz substrate, or a substrate made of a synthetic resin such as plastic or acrylic.

17. (Canceled)

18. (Original) The method for manufacturing a thin film integrated circuit according to claim 2,

wherein a mounting position of each of the two thin film integrated circuits X satisfies  $(1/2) \cdot D - 30 \text{ } \mu\text{m} < X < (1/2) \cdot D + 30 \text{ } \mu\text{m}$  when a thickness of a mount article is denoted by D.

19. (Original) The method for manufacturing a thin film integrated circuit according to claim 3,

wherein a mounting position of each of the two thin film integrated circuits X satisfies  $(1/2) \cdot D - 30 \text{ } \mu\text{m} < X < (1/2) \cdot D + 30 \text{ } \mu\text{m}$  when a thickness of a mount article is denoted by D.

20. (Canceled)

21. (Original) The method for manufacturing a thin film integrated circuit according to claim 3,

wherein the antenna is attached to the two thin film integrated circuits by an anisotropic conductor, an ultrasonic adhesive, or an ultraviolet curing resin.

22. (Original) The method for manufacturing a thin film integrated circuit according to claim 5,

wherein the antenna is attached to the two thin film integrated circuits by an anisotropic conductor, an ultrasonic adhesive, or an ultraviolet curing resin.

23. (Canceled)

24. (Original) The method for manufacturing a thin film integrated circuit according to claim 3,

wherein the antenna is formed by a method selected from the group consisting of a droplet discharge method, a sputtering method, a printing method, a plating method, a photolithography method, an evaporation method using a metal mask, and a combination thereof.

25. (Original) The method for manufacturing a thin film integrated circuit according to claim 5,

wherein the antenna is formed by a method selected from the group consisting of a droplet discharge method, a sputtering method, a printing method, a plating method, a photolithography method, an evaporation method using a metal mask, and a combination thereof.

26. (Canceled)

27. (Original) The method for manufacturing a thin film integrated circuit according to claim 2,

wherein the separation layer is an amorphous semiconductor, a semi-amorphous semiconductor, a microcrystalline semiconductor, or a crystalline semiconductor.

28. (Original) The method for manufacturing a thin film integrated circuit according to claim 3,

wherein the separation layer is an amorphous semiconductor, a semi-amorphous semiconductor, a microcrystalline semiconductor, or a crystalline semiconductor.

29. (Canceled)

30. (Original) The method for manufacturing a thin film integrated circuit according to claim 2,

wherein the two thin film integrated circuits have a thickness of 0.3  $\mu\text{m}$  to 3  $\mu\text{m}$ .

31. (Original) The method for manufacturing a thin film integrated circuit according to claim 3,

wherein the two thin film integrated circuits have a thickness of 0.3  $\mu\text{m}$  to 3  $\mu\text{m}$ .

32. (Canceled)

33. (Original) The method for manufacturing a thin film integrated circuit according to claim 2,

wherein the two thin film integrated circuits are 5 mm squared or less.

34. (Original) The method for manufacturing a thin film integrated circuit according to claim 3,

wherein the two thin film integrated circuits are 5 mm squared or less.

35. (Canceled)

36. (Original) The method for manufacturing a thin film integrated circuit according to claim 2,

wherein each of the two thin film integrated circuits includes a semiconductor film having a hydrogen concentration of  $1 \times 10^{19} / \text{cm}^3$  to  $5 \times 10^{20} / \text{cm}^3$ .

37. (Original) The method for manufacturing a thin film integrated circuit according to claim 3,

wherein each of the two thin film integrated circuits includes a semiconductor film having a hydrogen concentration of  $1 \times 10^{19} / \text{cm}^3$  to  $5 \times 10^{20} / \text{cm}^3$ .

38. (Canceled)

39. (Original) The method for manufacturing a thin film integrated circuit according to claim 36,

wherein the semiconductor film has a thickness of  $0.2 \mu\text{m}$  or less.

40. (Original) The method for manufacturing a thin film integrated circuit according to claim 37,

wherein the semiconductor film has a thickness of  $0.2 \mu\text{m}$  or less.

41. (Canceled)

42. (Original) The method for manufacturing a thin film integrated circuit according to claim 36,

wherein the semiconductor film comprises a source region, a drain region, and a channel formation region and,

wherein the source region, the drain region, and the channel formation region are formed to be perpendicular to a bending direction of a mount article.

43. (Original) The method for manufacturing a thin film integrated circuit according to claim 37,

wherein the semiconductor film comprises a source region, a drain region, and a channel formation region and,

wherein the source region, the drain region, and the channel formation region are formed to be perpendicular to a bending direction of a mount article.

44. (Canceled)

45. (Original) The method for manufacturing a thin film integrated circuit according to claim 2,

wherein a thin film integrated circuit is formed by cutting the two thin film integrated circuits by a dicing, a scribing, or a laser cutting method.

46. (Original) The method for manufacturing a thin film integrated circuit according to claim 3,

wherein a thin film integrated circuit is formed by cutting the two thin film integrated circuits by a dicing, a scribing, or a laser cutting method.

47.-60. (Canceled)